REMARKS

The Examiner's Office Action of July 9, 2003 has been received and its contents reviewed. Applicants would like to thank the Examiner for the consideration given to the above-identified application.

By this Amendment, claims 1, 4, 6, 8, 30 and 36 have been amended, claim 33 has been cancelled, and new claims 39-45 have been newly added. Claims 10-27 were previously withdrawn from consideration and claim 32 was previously cancelled. Accordingly, claims 1-9, 28-31 and 33-45 are pending for consideration, of which claims 1 and 6 are independent. Applicants respectfully request reconsideration and allowance of all the pending claims.

Referring now to the detailed Office Action, claims 1-3, 6, 7, 29, 33, 34 and 38 are rejected under 35 U.S.C. 102(b) as being anticipated by US Patent No. 4,969,031 to Kobayashi. Also, claims 28 and 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kobayashi, in view of US Patent No. 6,093,951 to Burr, and claims 4, 5, 8, 9, 30, 31, 36 and 37 are rejected under 35 U.S.C. 103(a) as being unpatentable over alleged Admitted Prior art in view of Kobayashi and Burr. Applicant respectfully traverses these rejections, in view of the amendments provided above and the comments that follow below.

Kobayashi discloses three methods for forming a MOSFET. The first method (see col. 2, line 61 to col. 3, line 54) is performed by melting and regrowing a principal surface of a Silicon single-crystal substrate. The second method (see col. 3, line 56 to col. 5, line 50) comprises adding an impurity such as Boron or Phosphorus having a smaller covalent radius than Silicon to an active layer in which a semiconductor element of a Silicon single-crystal layer is to be formed, so as to form a tensile strain in the active layer. The third method (see col. 5, line 5 1 to col. 6, line 5) is performed on the principle surface of a Si single-crystal substrate with which Indium, having a larger covalent radius than that of silicon, is doped at about $10^{19}cm^{-3}$. A Silicon crystal layer containing boron as an impurity at a density of $10^{16}cm^{-3}$ is then grown. Accordingly, a growth layer (active layer) having a tensile strain is formed.

To the contrary, the semiconductor device recited in claim 1 of the present invention includes a MIS transistor formed on a semiconductor substrate. The semiconductor substrate is an epitaxial semiconductor substrate having an epitaxial region formed by epitaxial

growing silicon on a silicon substrate. The MIS transistor includes a gate electrode formed above the epitaxial region with a gate insulating film sandwiched therebetween and a diffusion layer formed in the epitaxial region, by using a dopant ion having a relatively large mass number, and the diffusion layer is formed shallower than the epitaxial region. By forming the diffusion layer of the MIS transistor in the epitaxial region in the aforesaid manner, occurrence of defects derived from heavy ions can be suppressed. Hence, the semiconductor device having high driving power can be refined with a leakage current suppressed. Applicant respectfully submits that Kobayashi fails to disclose or suggest this combination of features.

For example, Kobayashi fails to disclose or suggest an MIS transistor formed on a semiconductor substrate wherein said semiconductor substrate is an epitaxial semiconductor substrate and that the epitaxial region is formed by epitaxial growing silicon on the silicon substrate, as now set forth in independent claim 1. Instead, Kobayashi, discloses forming MOSFETS by melting through the use of a laser beam 2 and regrowing (by natural cooling) a principal surface of a silicon single-crystal substrate in one embodiment (see col. 2, line 61 to col. 3, line 54). Nowhere is it disclosed that an epitaxial region is formed by epitaxial growing silicon or that an MIS transistor is formed on a semiconductor substrate wherein said semiconductor substrate is an epitaxial semiconductor substrate, as described in independent claim 1.

Additionally, Applicant respectfully submits that Kobayashi does not disclose a diffusion layer formed in said expitaxial region, by using a dopant ion having a relatively large mass number, as recited in independent claim 1. Instead, Kobayashi discloses employing a diffusion layer formed in the active layer by using a dopant ion having a relatively small mass number (see col. 3, line 56 to col. 5, line 50) and utilized boron, having a relatively small mass number, as a dopant ion (see col. 5, line 5 1 to col. 6, line 5). Thus, Kobayashi does not use a dopant ion having a diffusion layer formed in said expitaxial region, by using a dopant ion having a relatively large mass number, as recited in independent claim 1. For these reasons, Applicant respectfully requests reconsideration and withdrawal of the rejection.

Additionally, Applicant respectfully submits that the Burr, employed to disclose a specific ion dose for doping, and Admitted Prior Art, used to disclose a MIS transistor, do not

solve the deficiencies of the Kobayashi patent.

Independent claim 6, as currently amended, is directed to a semiconductor device that includes a MIS transistor formed on a semiconductor substrate. The semiconductor substrate is composed of silicon and has a main surface of {110}-orientation. The MIS transistor includes a gate electrode formed above the semiconductor substrate with a gate insulating film sandwiched therebetween and a diffusion layer is formed, by using a dopant ion having a relatively large mass number, in the semiconductor substrate. As a result, occurrence of defects derived from heavy ions can be suppressed. Hence, the semiconductor device having high driving power can be refined with a leakage current suppressed. Applicant respectfully submits that Kobayashi does not disclose or suggest the combination of features provided in independent claim 6.

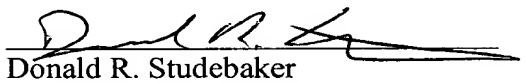
For example, Applicant respectfully submits that Kobayashi fails to disclose or suggest a MIS transistor that includes a diffusion layer formed by using a dopant ion having a relatively large mass number, as now set forth in independent claim 6. Instead, Kobayashi discloses employing a diffusion layer formed in the active layer of a MOSFET by using a dopant ion having a relatively small mass number (see col. 3, line 56 to col. 5, line 50) and utilizing boron, having a relatively small mass number, as a dopant ion (see col. 5, line 5 1 to col. 6, line 5). Thus, Kobayashi does not disclose or suggest a MIS transistor that includes a diffusion layer formed by using a dopant ion having a relatively large mass number, as now set forth in independent claim 6. Thus, Applicant respectfully requests reconsideration and withdrawal of the rejection.

Additionally, Applicant respectfully submits that the Burr, employed to disclose a specific ion dose for doping, and Admitted Prior Art, used to disclose a MIS transistor, do not solve the deficiencies of the Kobayashi patent.

Also, claims 2-5, 7-9, 28-31 and 34-45 are dependent claims and are allowable for at least the same reasons as discussed with respect to independent claims 1 and 6, as well as for reasons of their own.

While the present application is now believed to be in condition for allowance, should the Examiner find some issue to remain unresolved, or should any new issues arise which could be eliminated through discussions with Applicant's representative, then the Examiner is invited to contact the undersigned by telephone in order that the further prosecution of this application can thereby be expedited.

Respectfully submitted,



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